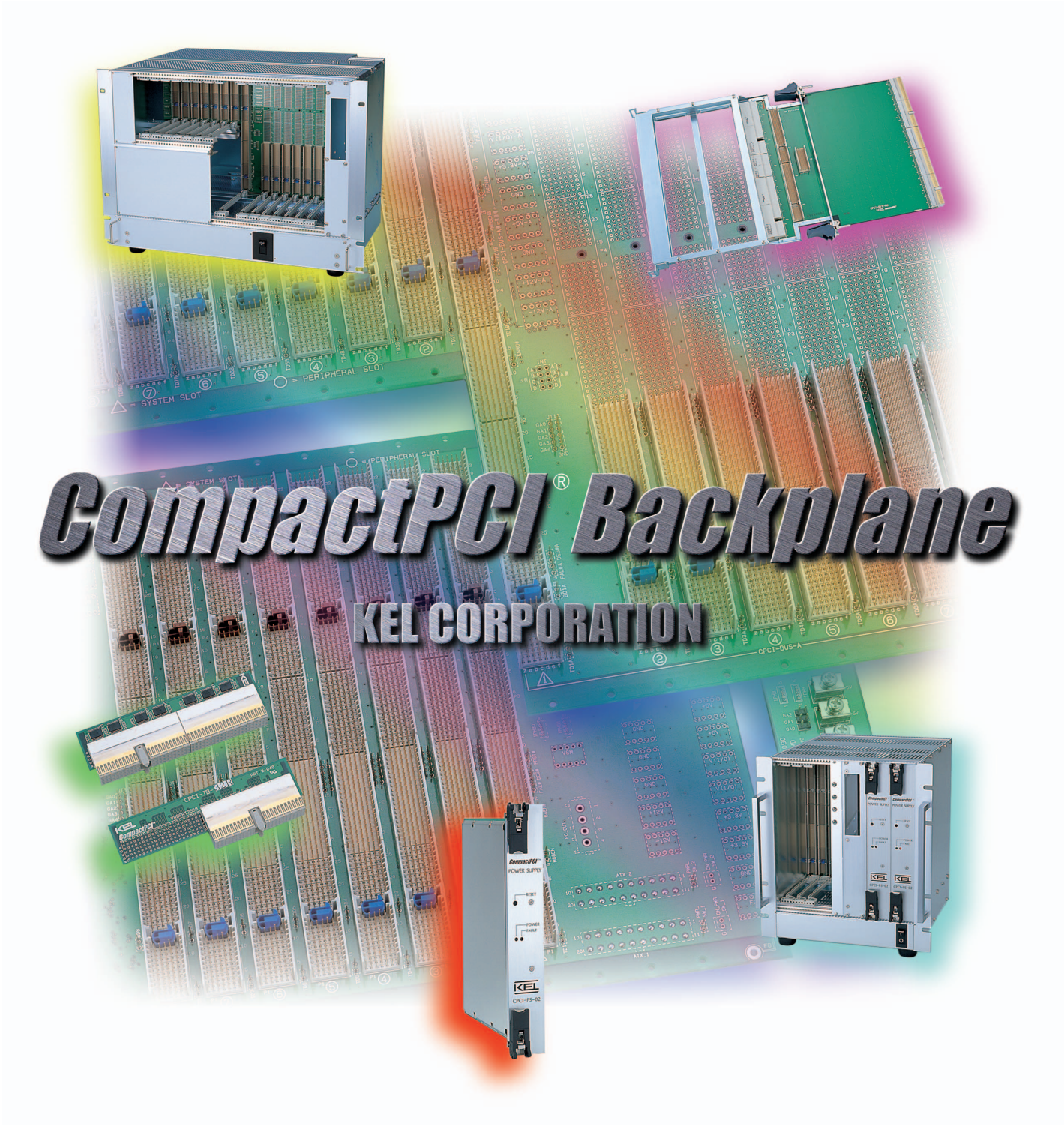
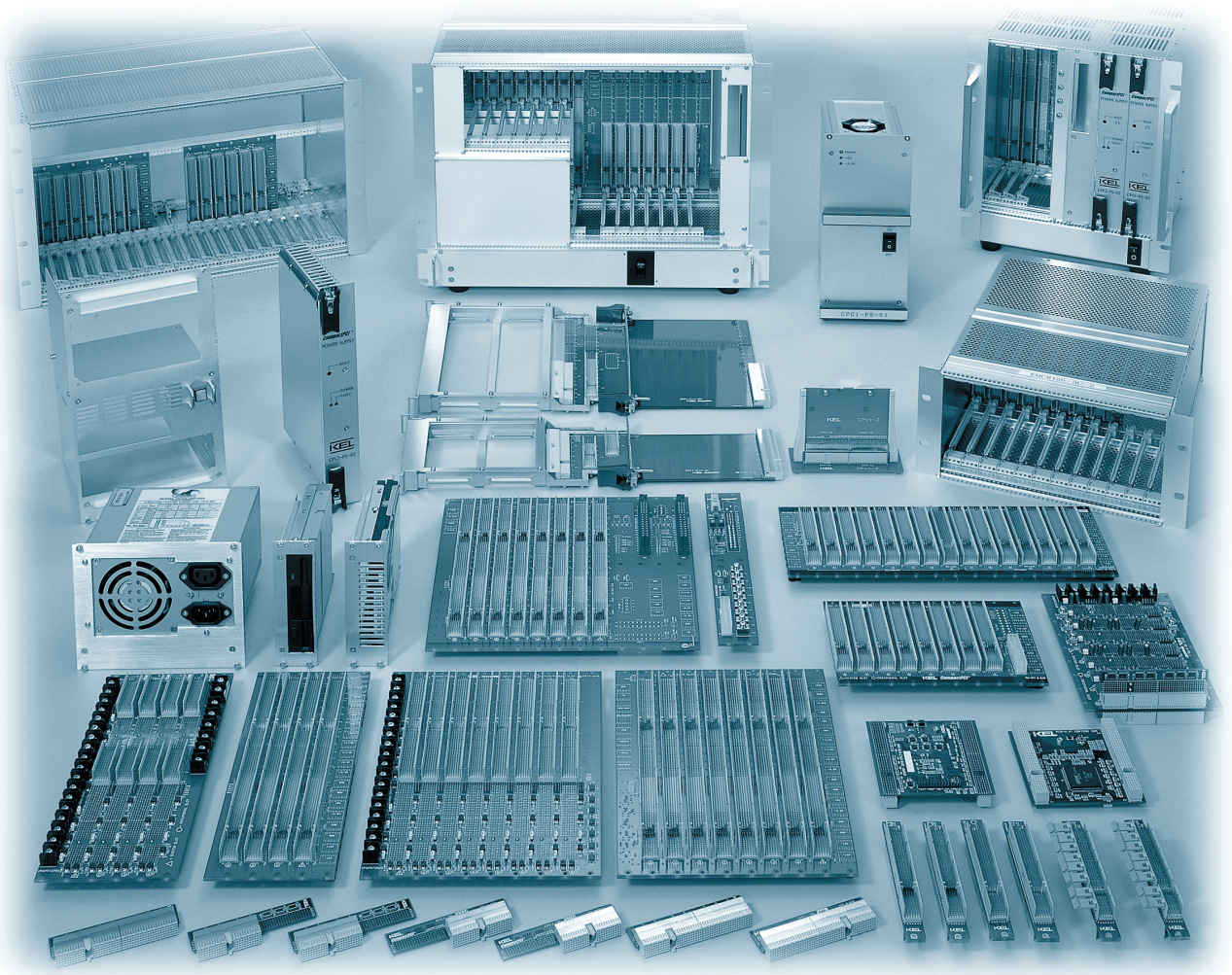

CompactPCI® Backplane
KEL CORPORATION

KEL



R3.0 Compliant Backplane
Dual Type Packet Switching Backplane
Centerized Dual Type Star Fabric Backplane
R2.1 Compliant 3U Backplane
Termination Implementing Backplane
ATX Power Supply Connector Equipped Backplane
Hot Swap Compatible 6U Backplane
Computer Telephony Compatible 6U Backplane
Bridge Board Compatible 3U Backplane (15 Slots)
Pallet-Type Bridge Board
Dual-Bus Compatible 6U Backplane
Plug-In Power Supply Compatible 6U Backplane
Extension Board for CompactPCI Boards
Termination Board
Rear I/O Adapter
CompactPCI System Rack
CompactPCI Dual-Bus System Rack
CompactPCI Plug-In Power Supply Unit
Slot-In Four-Output Power Supply Unit
Rack-Mount-Type 300W/145W Power Supply Unit
Disc Unit Chassis
CompactPCI Subrack and Connectors

CompactPCI® Backplane

What is CompactPCI™

CompactPCI is a specification developed from the Peripheral Component Interconnect (PCI) Specification (Revision 2.1 and later versions) for industrial embedded computers that require higher mechanical robustness than desktop PCI-based systems. Supported by the PCI Industrial Computers Manufacturers Group (PICMG), the CompactPCI specification reflects the group's aim of developing specifications to provide an optimum system for use in industrial computing applications using industry-standard components and high-performance connector technologies. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low-cost PCI components to be used in a mechanical form factor suitable for rugged environments. CompactPCI is an open specification controlled by the PICMG.
KEL Corporation offers high-quality CompactPCI-compliant products for embedded applications in variety of industrial fields.
CompactPCI is a trademark of PCI Industrial Computers Manufacturers Group.

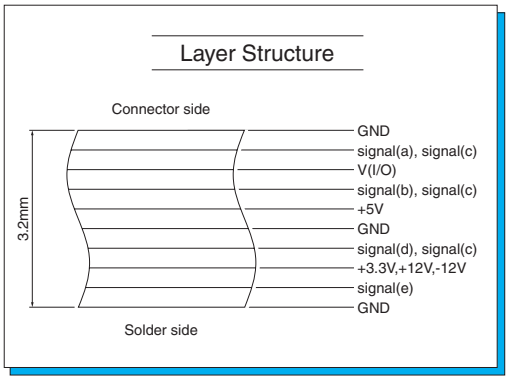
KEL CORPORATION

Common Specifications of KEL Compact PCI (CPCI) Series Products

The basic design of every KEL CPCI Series product completely satisfies all the PICMG's backplane-related requirements. For backplane features not defined by the specifications but left to backplane manufacturers' discretion, KEL can provide optimum solutions taking into account customers' needs and expected expansion of specifications. Note that KEL will enhance its products' specifications and add new products as the PICMG continues to establish standards.

Basic Specifications Common to all KEL CPCI Series Products

● PWB
- Material : FR-4 (UL grade)
- Finish : Solder leveler (SC method)
- Board thickness : 3.2mm
- Number of layers : 10
- Characteristic impedance 65Ω ±10%(test coupon value)
- Decoupling capacitor layout conforms to CompactPCI Specification requirements.
  Layer configuration and pattern layout are optimized.



● Terminals, Connectors, and Other Implementation
- Power supply terminal ...KEL FT-10-4 (rated current:20A per pin)
- V (I/O) ...Default set to 5V by short bar across power pins
- Jumper terminal ...KEL DSP Series
- Connectors ...KEL CP Series connectors and other manufacturers' connectors that conform to CompactPCI Specification (with KEL connectors used wherever possible for cost savings and quick delivery)
- Keying ...Keying mechanism provided for 5V setting (or 3.3V setting if requested by customer) at time of shipment

● Compliance with IEEE 1101.11 Standard
- KEL can tailor products for customers using a board thickness and shroud bottom thickness that comply with the IEEE1101.11 standard. Please contact your local sales office to discuss your needs.

Jumper Setting and Lead Specifications

● Miscellaneous Signals
- M66EN Enables selection of a 33MHz or 66MHz clock frequency. The default setting (jumper switch) is 33MHz.
- 64EN# Allows the system to identify 32-bit and 64-bit data . The default setting (jumper switch) is 64-bit.
- BD_SEL With a hot-swappable board,these signals are used to implement hardware connection control. The pins for these signals are marked BD1-BD8, and they are connected to ground before the board is shipped from the factory.
- PRST# Used to externally reset the system slot.
- RST Used to reset all PCI resources.

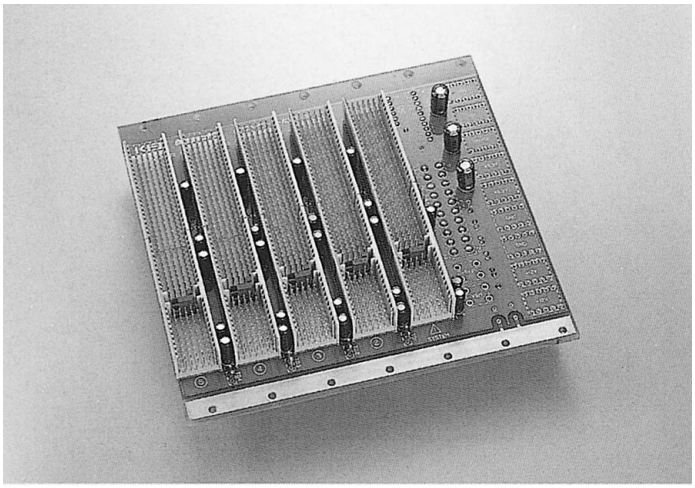
● Power Supply Status Related Signals
- FAL# Used to inform the system slot of a power fault.
- DEC# Used to inform the system slot of a drop in power output level.

● JTAG-Related Signals
- GA0-GA4 These are JTAG geographic address designation signals, and they can be jumper-selected. The pins for these signals are identified as JT1-JT8 (GA0-GA4), with the marks printed between slots. (These marks are PR1-PR8 under the PICMG2.0R2.1 specification.)
- TDI/TDO These signals are used as JTAG commands and for serial shift of data. Their pins are marked TD1-TD8. (These marks are JP01-JP08 under the PICMG2.0R2.1 specification.)
- TRST# Used to initialize the TAP controller of PCI resources (device ICs with PCI bus interfaces.)

* For information on the specifications and features of products, please refer to the following pages or contact KEL directly.

KEL Custom-Made CompactPCI Products

In addition to the standard CompactPCI products shown in this catalogue, KEL can also supply CompactPCI items tailored to customers' special needs. Irrespective of compliance or non-compliance with standards, KEL can rapidly design, manufacture, and supply backplane and rack products to customers' specifications and deliver them in a rack-assembled form. We offer such products under the KEL Custom Rack (KCR) Series brand. For further details of KCR Series products, please contact your local sales office.



Relevant Specification

- PICMG2.1R1.0
- PICMG2.5R1.0
- ECTF H.110

Product Features

- A computer telephony coding key is implemented in connector P4.
- Used to construct computer telephony systems.

Product Specification

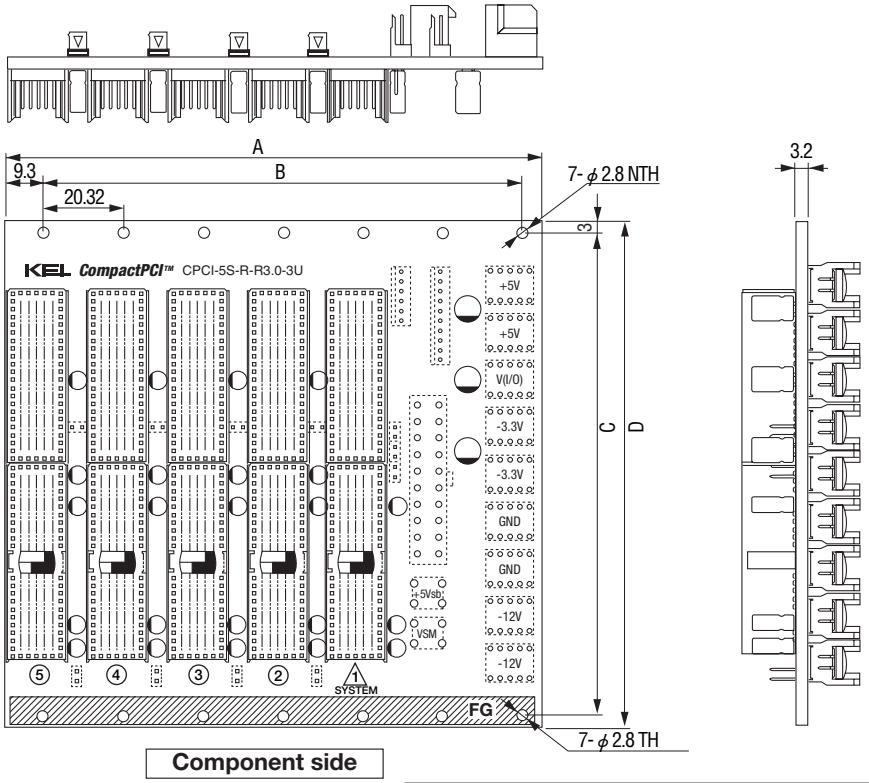
- Connectors P1 and P2 are equivalent to those of the CPCI-H backplane.
- Connector P3 is assigned to user-defined I/Os.
- Connector P4 is assigned to the H.110 bus.
- Connector P5 is assigned to user-defined I/Os for the H.110 bus.
- Eight-slot backplanes each have a pre-mounted diode array.
- A telecommunication power supply pin is provided at P4.
- Satisfies the insulation requirements of the specifications.

ORDER CODE

CPCI-5S-R-R3.0-□U

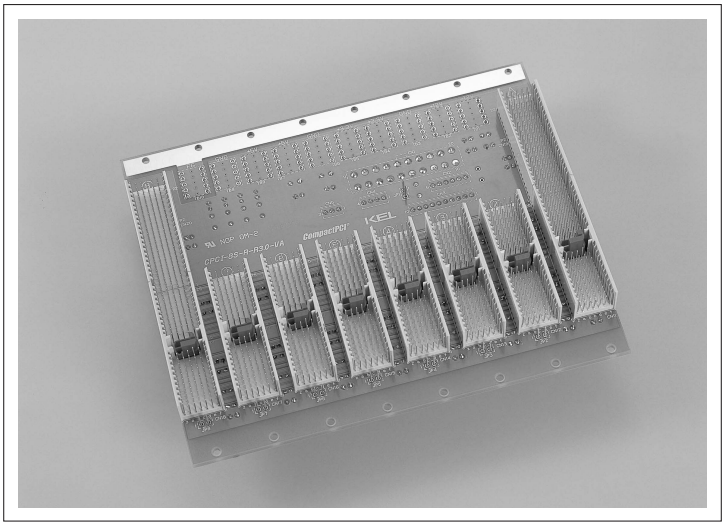
- 5S: Type : PICMG2.5R1.0 (Compliant telephony-bus-compatible backplane)
- R: No. of slots — 4 : Four 8 : Eight
- R: System slot position — R : Right
- R3.0: System slot position — R : Right
- □U: System slot position — R : Right

Unit:mm(inch)



Component side

No. of slots	Order Code	Dimension A	Dimension B	N
4	CPCI-C-4S-R	117.16(4.613)	101.60(4.000)	12
8	CPCI-C-8S-R	198.44(7.813)	182.88(7.200)	20



Relevant Specification

- PICMG2.1R2.1
- PICMG2.6D0.1

Product Features

- The segment configuration is as follows
  Full-slot connector type (F-type) : System slot 1
  : Peripheral slots 13
  Standard connector type (S-type) : System slot 1
  : Peripheral slots 12
  The S-type has no front bridge board insertion slot .
  Except for special applications, the F-type backplane is recommended.
- Backplane is designed for use with the CPCI-B/B Series bridge boards (see page M-11).
- Backplane is not hot-swappable as it is designed to be PICMG2.0R2.1 specification.

ORDER CODE

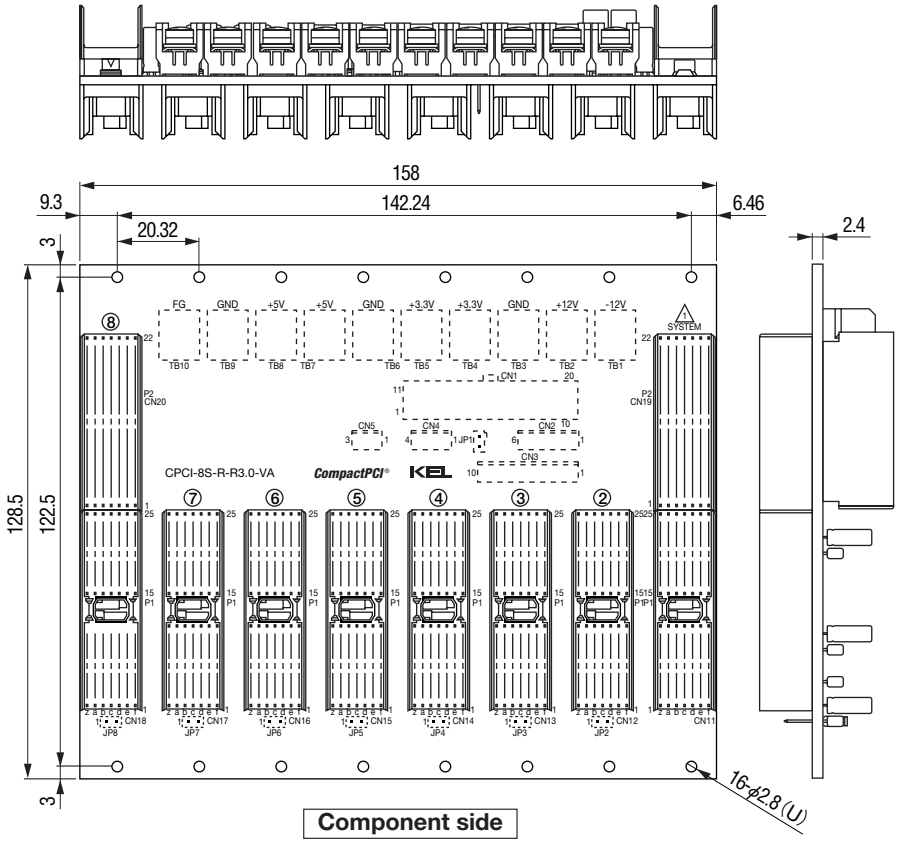
CPCI-8S-R-R3.0-VA-

- System slot position R : Right
- System slot position R : Right
- System slot position R : Right
- No. of slots 4 : Four 8 : Eight
- Type : PICMG2.5R1.0 (Compliant telephony-bus-compatible backplane)

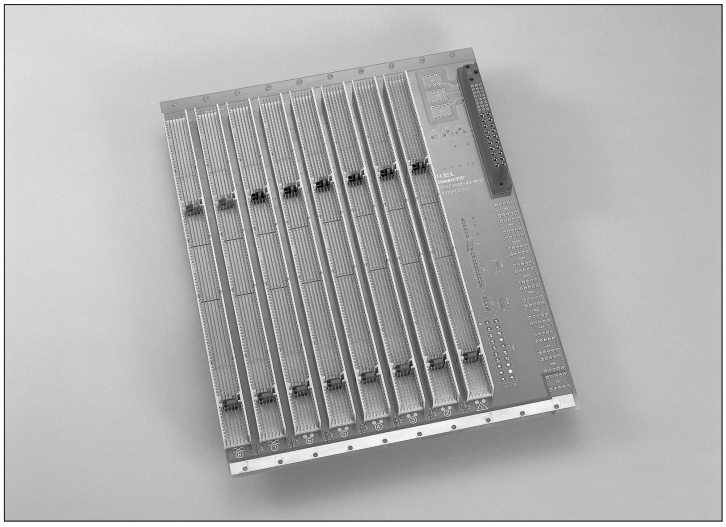
Product Specification

- Designed for use with the CPCI-B/B Series bridge boards (see page M-11)
- 3U board size
- Satisfies the clock routing requirements of the PICMG2.0R2.1 specification.
- The power supply layer is split into primary and secondary sides.
- The ground layer is common to the primary and secondary sides.
- 15 physical slots

Unit:mm(inch)



Component side



Relevant Specification

- PICMG2.0R2.1

Product Features

- Designed for use with ATX-specification power supply.

Product Specification

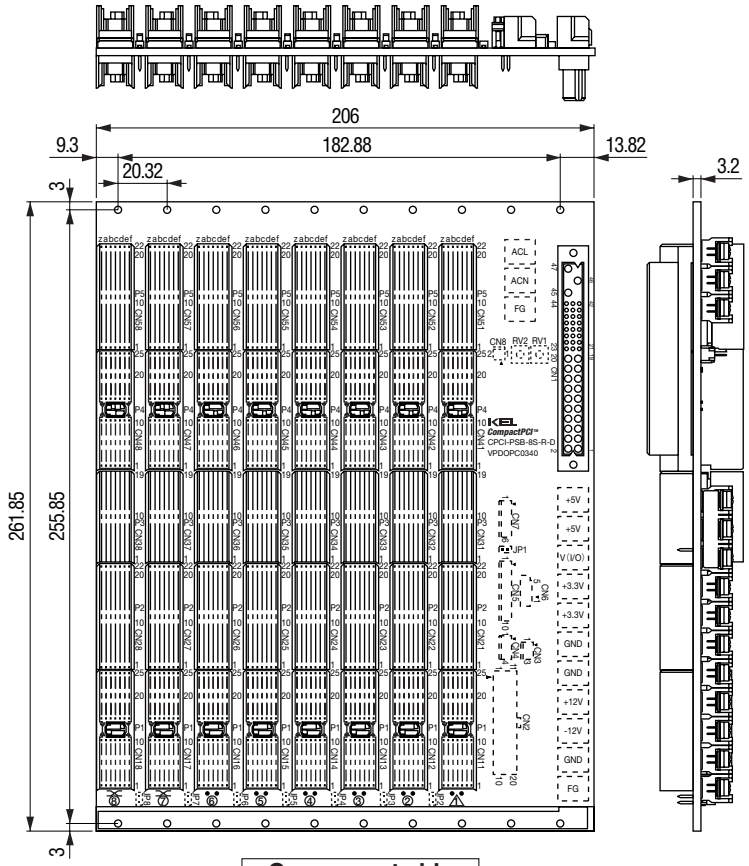
- Basic parts of this product are the same as those of the R2.1 compliant 3U backplane (CPCI-□S-□-R2.1).
- Fitted with a connector for an ATX power supply.

ORDER CODE

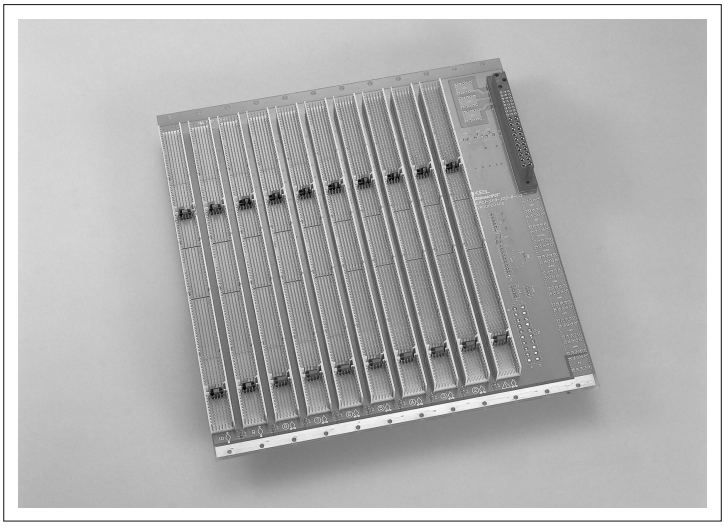
CPCI-PSB-8S-R-D

- D: System slot position R : Right
- R: System slot position R : Right
- 8S: No. of slots 4 : Four 8 : Eight
- PSB: Type : PICMG2.5R1.0 (Compliant telephony-bus-compatible backplane)

Unit:mm(inch)



Component side



Relevant Specification

- PICMG2.1R2.1
- PICMG2.6D0.1

Product Features

- The segment configuration is as follows
  Full-slot connector type (F-type) : System slot 1
  : Peripheral slots 13
  Standard connector type (S-type) : System slot 1
  : Peripheral slots 12
  The S-type has no front bridge board insertion slot .
  Except for special applications, the F-type backplane is recommended.
- Backplane is designed for use with the CPCI-B/B Series bridge boards (see page M-11).
- Backplane is not hot-swappable as it is designed to be PICMG2.0R2.1 specification.

ORDER CODE

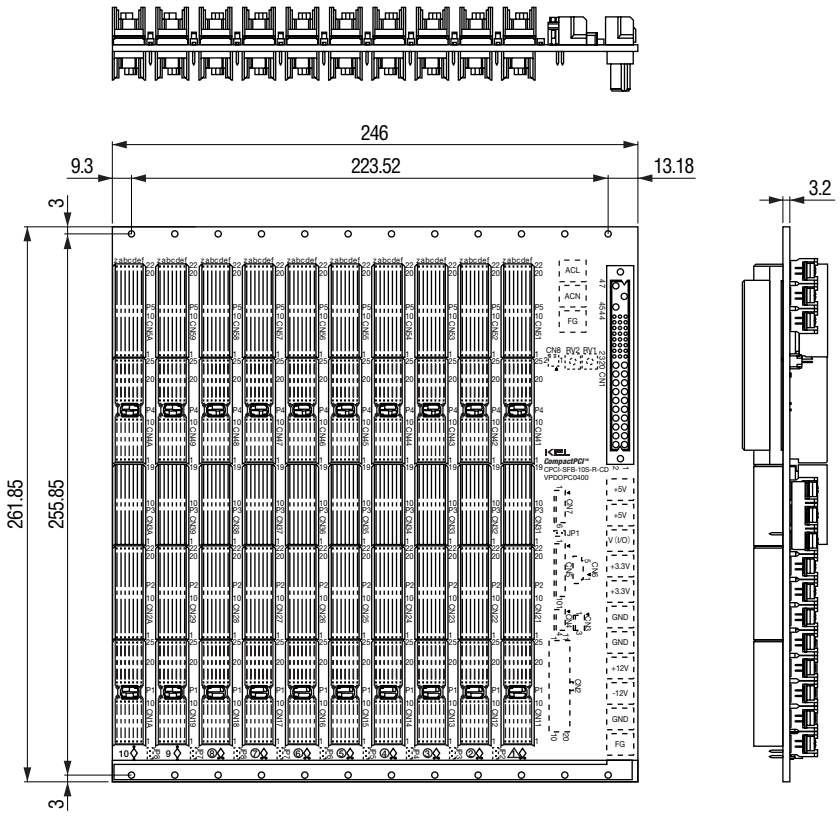
CPCI-SBF-10S-R-CD

- System slot position R : Right
- System slot position R : Right
- No. of slots 4 : Four 8 : Eight
- Type : PICMG2.5R1.0 (Compliant telephony-bus-compatible backplane)

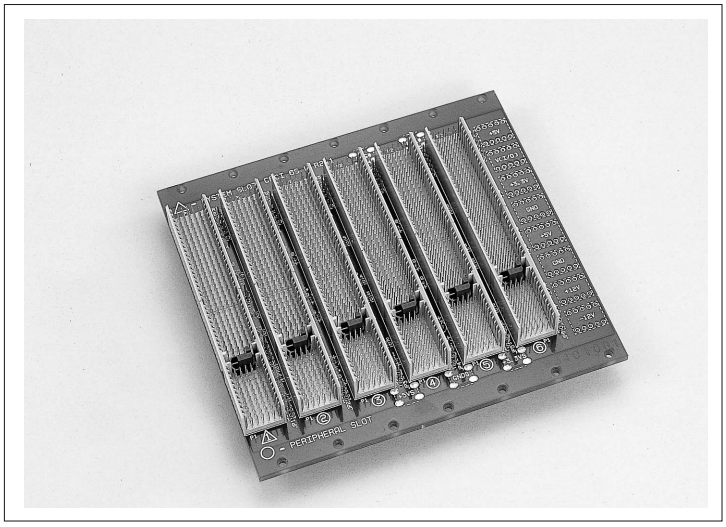
Product Specification

- Designed for use with the CPCI-B/B Series bridge boards (see page M-11)
- 3U board size
- Satisfies the clock routing requirements of the PICMG2.0R2.1 specification.
- The power supply layer is split into primary and secondary sides.
- The ground layer is common to the primary and secondary sides.
- 15 physical slots

Unit:mm(inch)



A 3U backplane compliant with CompactPCI core specification R2.1



Relevant Specification

- PICMG2.0R2.1

Product Features

- 3U size
- Wired for 64-bit signaling system
- Five clock routings
- Sensing terminals implemented

Product Specification

- Conforms to the CompactPCI Specification Revision 2.1 (The core specification for the CompactPCI bus.)

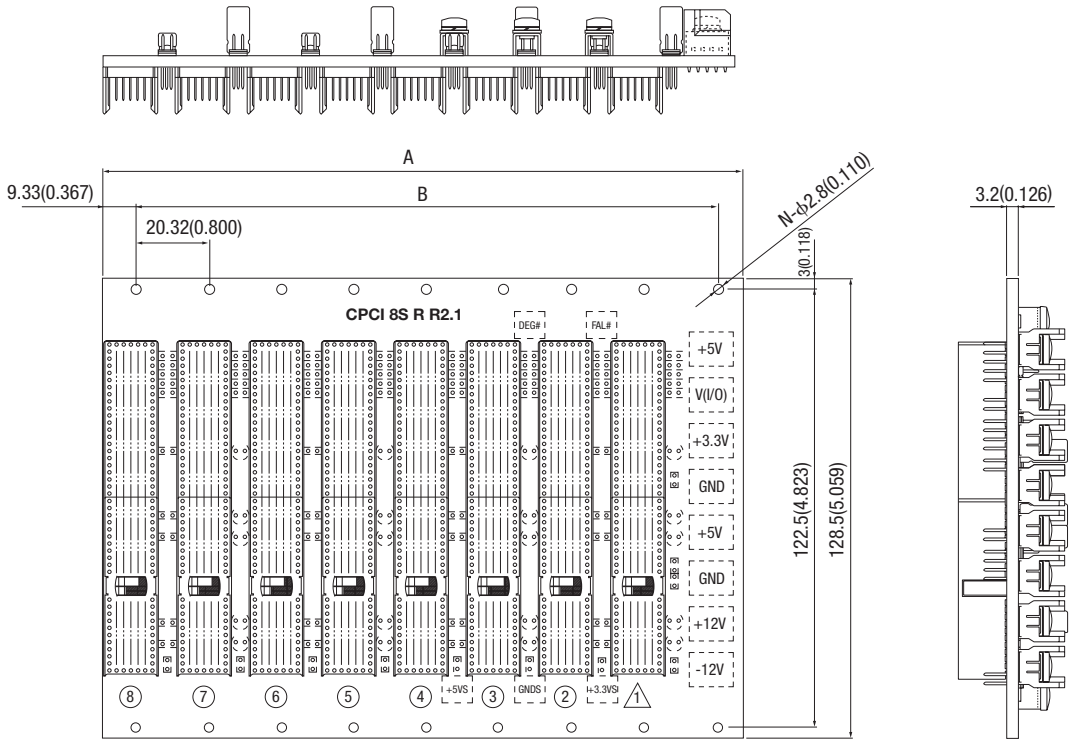
* KEL can also provide 3U Backplane for PICMG2.0R1.0-compliant.

ORDER CODE

CPCI-□S-□-R2.1

- Type : PICMG2.0R2.1 compliant 3U backplane
- System slot position R : Right L : Left
- No. of slots 4 : Four 6 : Six 8 : Eight

Unit:mm(inch)

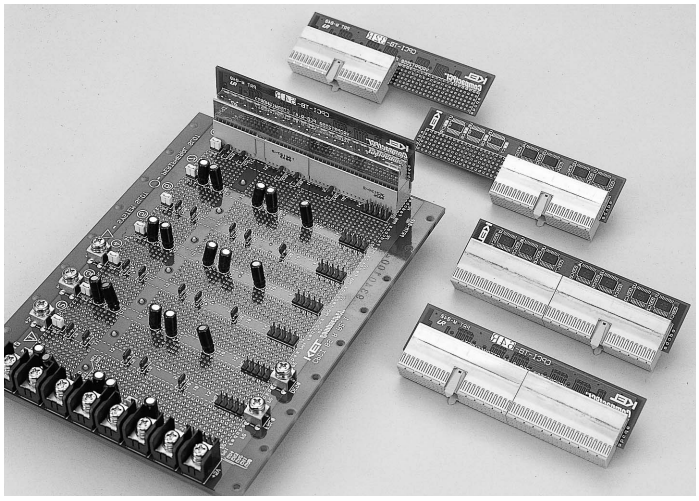


Component side

No. of slots	Order Code	Dimension A	Dimension B	N
4	CPCI-4S-L(R)-R2.1	96.84(3.813)	81.28(3.200)	10
6	CPCI-6S-L(R)-R2.1	137.48(5.413)	121.92(4.800)	14
8	CPCI-8S-L(R)-R2.1	178.12(7.013)	162.56(6.400)	18

Termination-Implementing Backplane

A backplane for implementing CPCI-TB Series termination boards



Relevant Specification

- PICMG2.0R2.1

Product Features

- Used for mounting termination boards.
- Designed for use with CPCI-TB Series termination board (see page M-15).

Product Specification

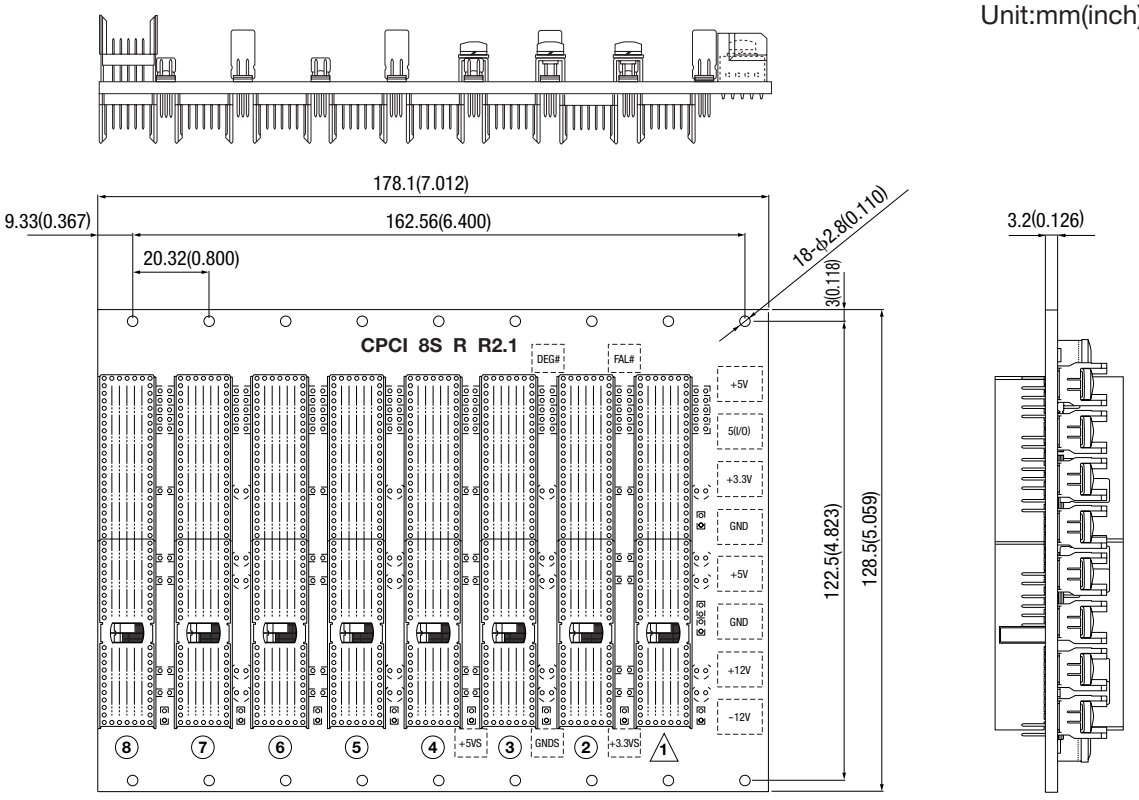
- Basic parts of this product are the same as those of the R2.1 compliant 3U backplane(CPCI-□S-□-R2.1).
- The rear shroud is mounted in slot#8.

ORDER CODE

CPCI-8S-□T-R 2.1

- Type : Backplane for implementing termination boards
- System slot position R : Right L : Left
- No. of slots 8 : Eight

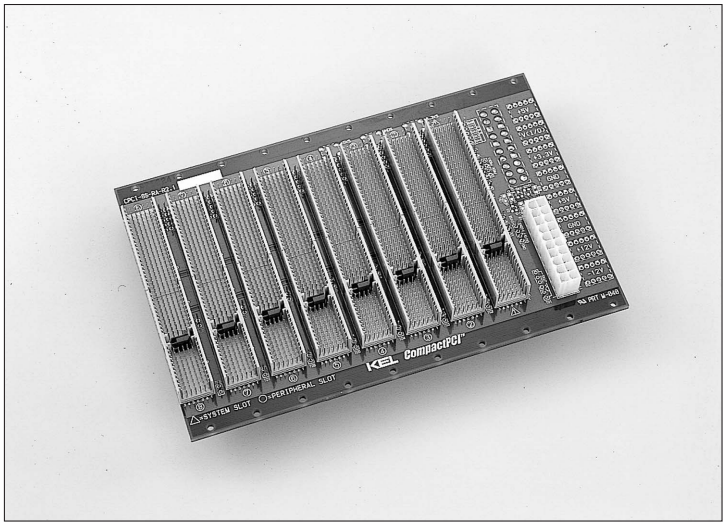
Unit:mm(inch)



Component side

Backplane Equipped with ATX Power Supply Connectors

A backplane with ATX connectors



Relevant Specification

- PICMG2.0R2.1

Product Features

- Designed for use with ATX-specification power supply.

Product Specification

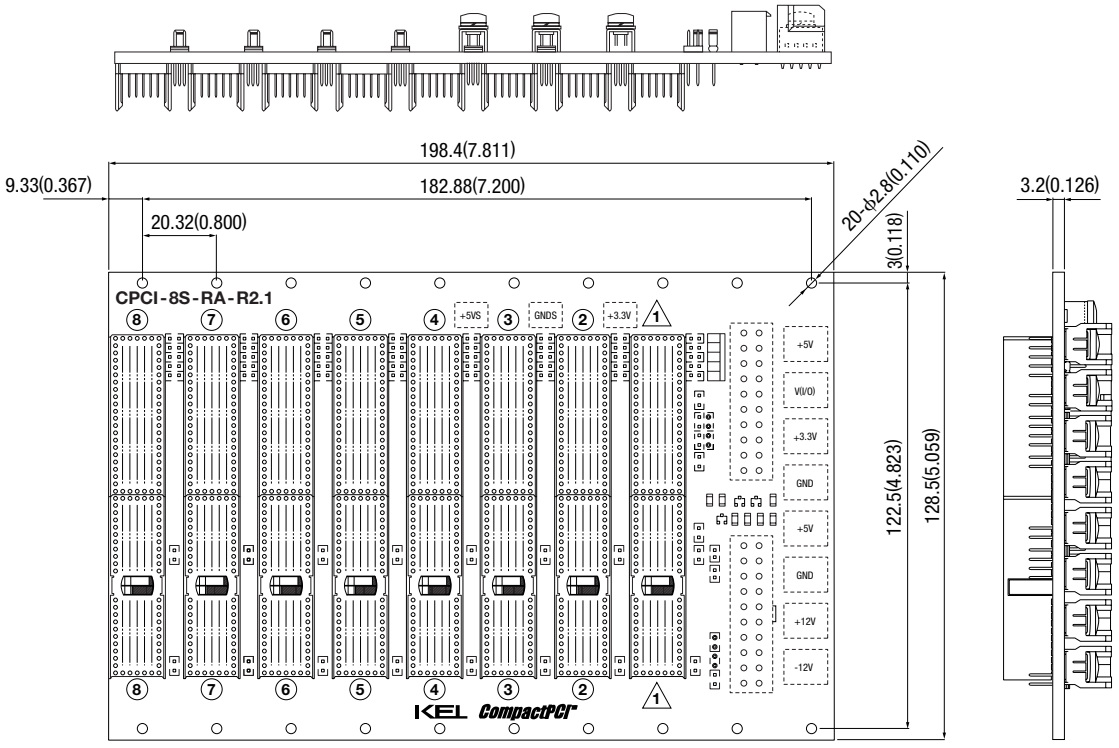
- Basic parts of this product are the same as those of the R2.1 compliant 3U backplane (CPCI-□S-□-R2.1).
- Fitted with a connector for an ATX power supply.

ORDER CODE

CPCI-8S-RA-R2.1

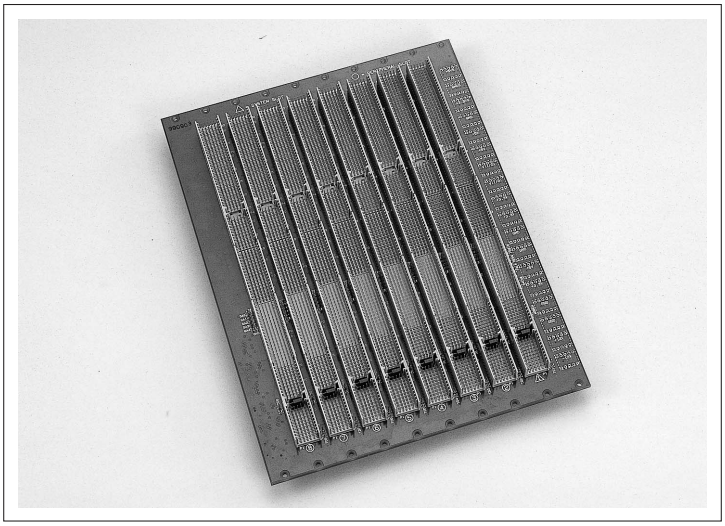
- Type
  : Backplane with ATX power supply connectors
- System slot position
  R : Right
- No. of slots
  8 : Eight

Unit:mm(inch)



Component side

A backplane with hot-swap capability



Relevant Specification

- PICMG2.0R1.0

Product Features

- Satisfying all hot-swap-related requirements of the PICMG2.1R1.0 specification, this backplane can be used for constructing a basic, full-slot, or high-availability system (fitted with appropriate boards).

* Please contact your local sales office for High Availability platform hardware specification.

Product Specification

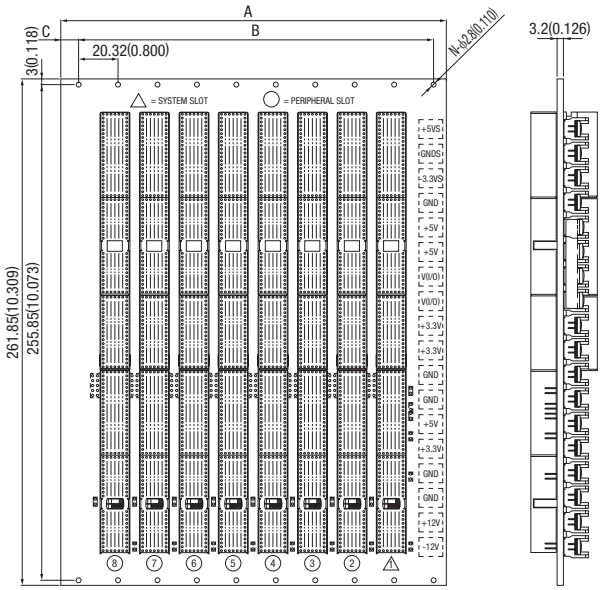
- The backplane is wired for 64-bit signaling.
- Seven clock routings (point to point) are provided.
- Connectors P3, P4, and P5 are assigned for user-defined I/Os.
- Backplane (CPCI-H-8S-□-□□) with 8slots has a premounted diode array.
- Three-level staged pins enable hot swapping.

ORDER CODE

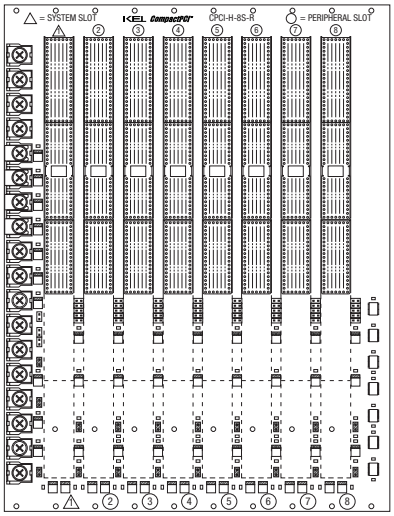
CPCI-H-□S-□-□□

- Backplane Size
  * 8 slots only
  Omit : 6U size 3U : 3U size
- System slot position
  R : Right L : Left
- No. of slots
  3 : Three 4 : Four 8 : Eight
- Type : Hot-swappable backplane compliant with PICMG2.7R1.0 specification

Unit:mm(inch)



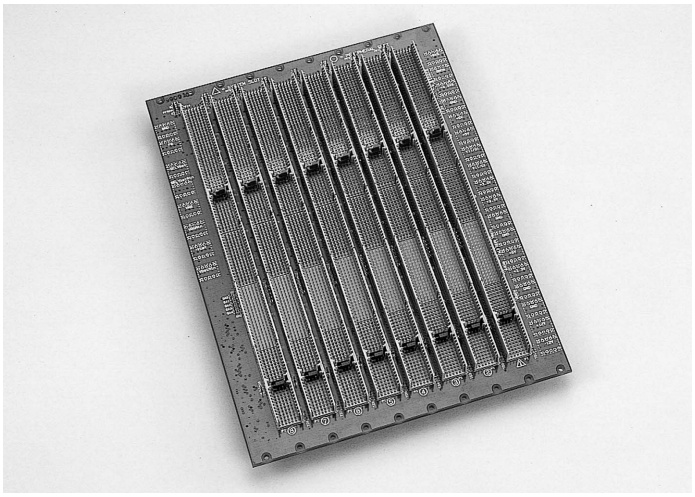
Component side



Solder side

No. of slots	Order Code	Dimension A	Dimension B	Dimension C	N
3	CPCI-H-3S-R	76.58(3.015)	60.96(2.400)	9.39(0.370)	8
4	CPCI-H-4S-R	107.00(4.213)	81.28(3.200)	19.49(0.767)	10
4	CPCI-H-4S-L	107.00(4.213)	81.28(3.200)	9.33(0.367)	10
8	CPCI-H-8S-R	198.44(7.813)	182.88(7.200)	9.33(0.367)	20
8	CPCI-H-8S-L	198.44(7.813)	182.88(7.200)	9.33(0.367)	20
8	CPCI-H-8S-R-3U	198.44(7.813)	82.88(3.263)	9.33(0.367)	20

A backplane compatible with telephony bus boards



Relevant Specification

- PICMG2.1R1.0
- PICMG2.5R1.0
- ECTF H.110

Product Features

- A computer telephony coding key is implemented in connector P4.
- Used to construct computer telephony systems.

Product Specification

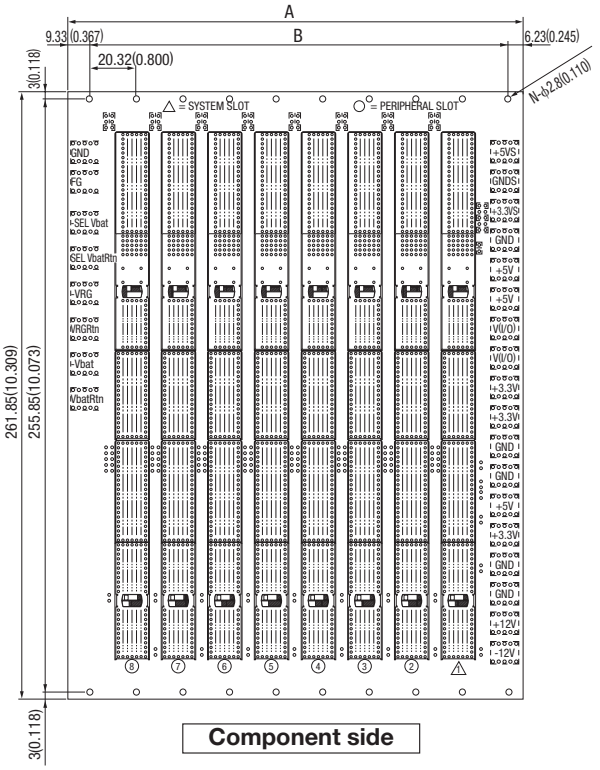
- Connectors P1 and P2 are equivalent to those of the CPCI-H backplane.
- Connector P3 is assigned to user-defined I/Os.
- Connector P4 is assigned to the H.110 bus.
- Connector P5 is assigned to user-defined I/Os for the H.110 bus.
- Eight-slot backplanes each have a pre-mounted diode array.
- A telecommunication power supply pin is provided at P4.
- Satisfies the insulation requirements of the specifications.

ORDER CODE

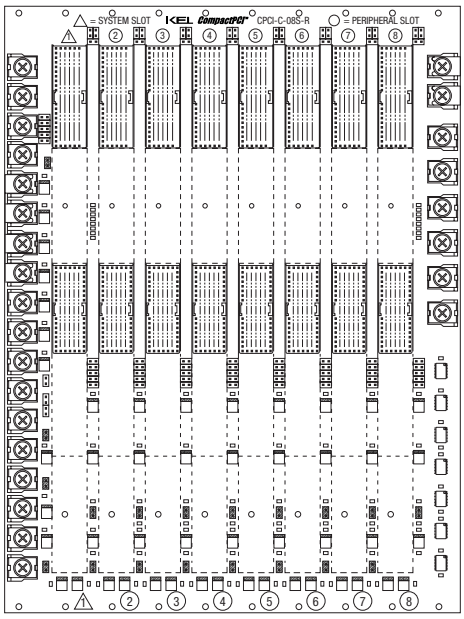
CPCI-C-□S-R

- System slot position
  R : Right
- No. of slots
  4 : Four 8 : Eight
- Type : PICMG2.5R1.0
  (Compliant telephony-bus-compatible backplane)

Unit:mm(inch)



Component side



Solder side

No. of slots	Order Code	Dimension A	Dimension B	N
4	CPCI-C-4S-R	117.16(4.613)	101.60(4.000)	12
8	CPCI-C-8S-R	198.44(7.813)	182.88(7.200)	20

Bridge-Board-Compatible 3U Backplane (15 Slots)

A backplane for CPCI-B/B Series bridge boards

Relevant Specification

- PICMG2.1R2.1
- PICMG2.6D0.1

Product Features

- The segment configuration is as follows
  Full-slot connector type (F-type) : System slot 1
  : Peripheral slots 13
  Standard connector type (S-type) : System slot 1
  : Peripheral slots 12
  The S-type has no front bridge board insertion slot .
  Except for special applications, the F-type backplane is recommended.
- Backplane is designed for use with the CPCI-B/B Series bridge boards (see page M-11).
- Backplane is not hot-swappable as it is designed to be PICMG2.0R2.1 specification.

ORDER CODE

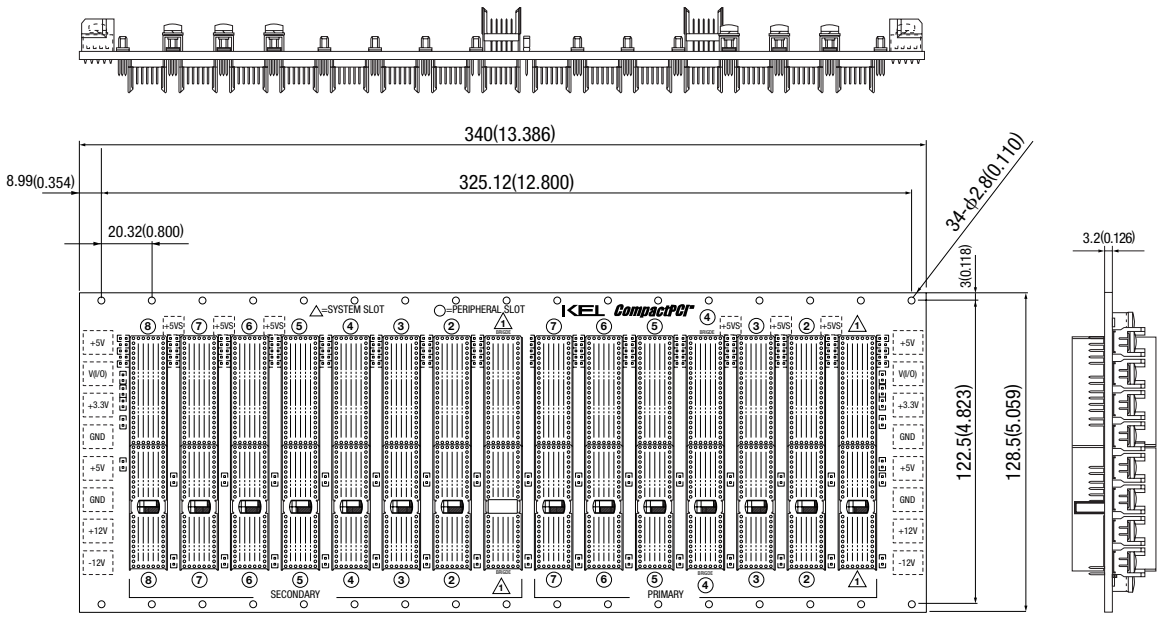
CPCI-B-15S-□-R

- System slot position
  R : Right
- Connector
  F : Full-function connector
  S : Standard connector
- No. of physical slots 15 : Fifteen
- Type : PICMG2.6D0.1-compliant
  (Bridge-Board-Compatible backplane)

Product Specification

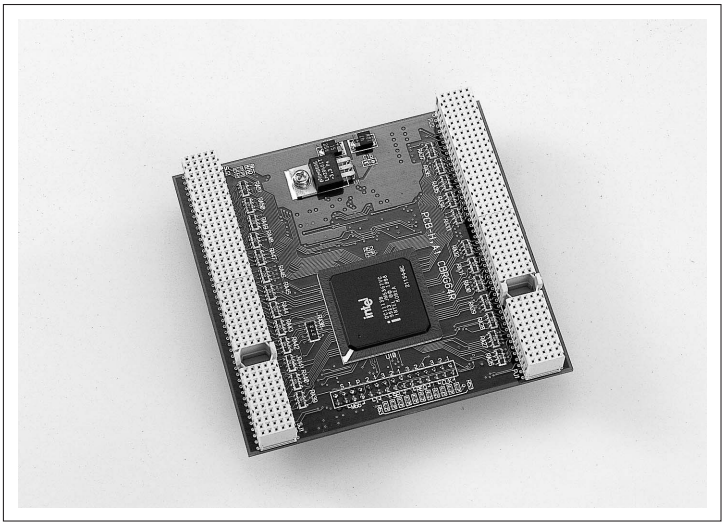
- Designed for use with the CPCI-B/B Series bridge boards (see page M-11)
- 3U board size
- Satisfies the clock routing requirements of the PICMG2.0R2.1 specification.
- The power supply layer is split into primary and secondary sides.
- The ground layer is common to the primary and secondary sides.
- 15 physical slots

Unit:mm(inch)



Component side

A pallet-type board with PCI bridge (ICs are mounted)



Relevant Specification

- PCI to PCI Bridge Specification Rev.1.0
- PICMG2.6D0.1

Product Features

- Designed for use with bridge-board-compatible 3U backplanes (CPCI-B-15S-□-R: see page M-10).
- Compatible with configurations in which multiple CPCI-□S-□-R2.1 backplanes are used (please consult KEL for possible configurations).
- Can also be used in combination with other backplane types or custom-made backplanes in accordance with system configuration requirements.

ORDER CODE

CPCI-B/B-64-□

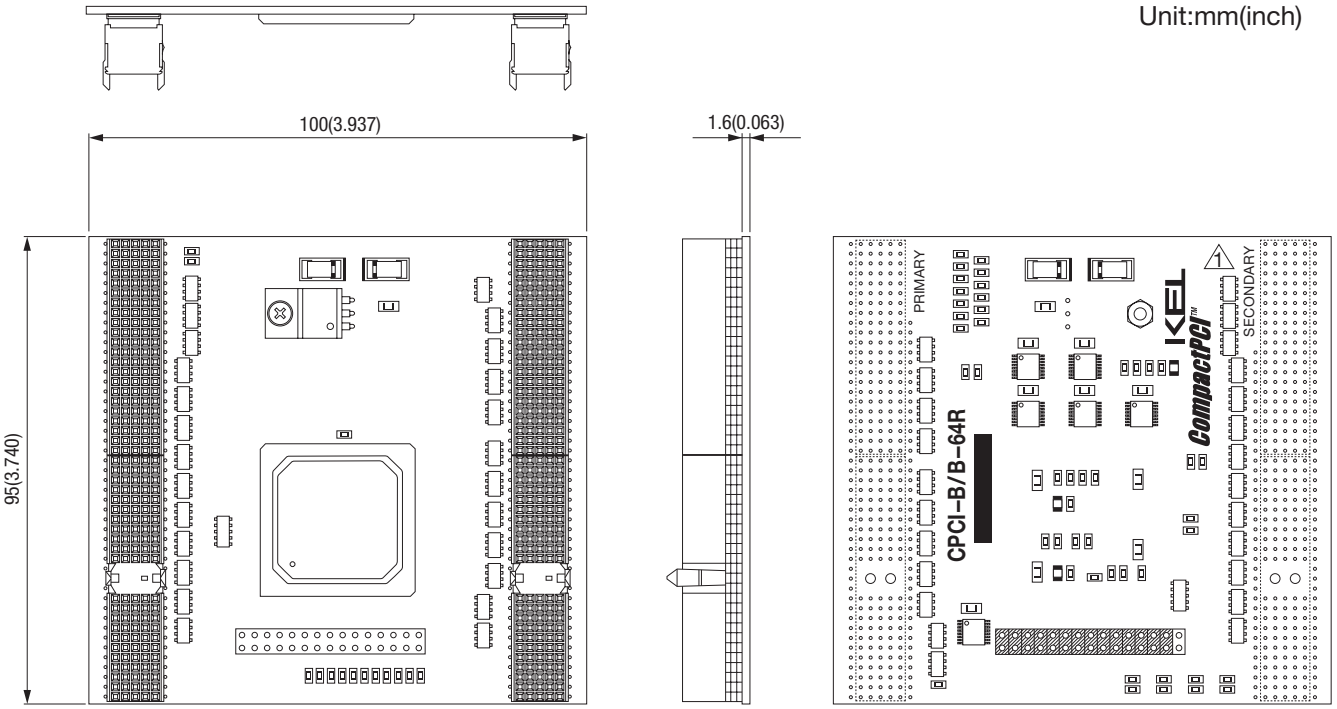
- □ : Primary side R : Right L : Left
- 64 : Applicable system 64 : 64-bit
- B/B : Type : PICMG2.6D0.1-compliant bridge board

Product Specification

- Primary side of bridge can be assigned to any desired slot by jumper setting.
- Bridge board is hot -swappable.
- Can be used with 5V power supplies.
- Versions of the board are available for both 32-bit and 64-bit systems.
- Primary-side slot can be shared with a daughter board.

*Connection capability for JTAG Signal is not incorporated.

Unit:mm(inch)

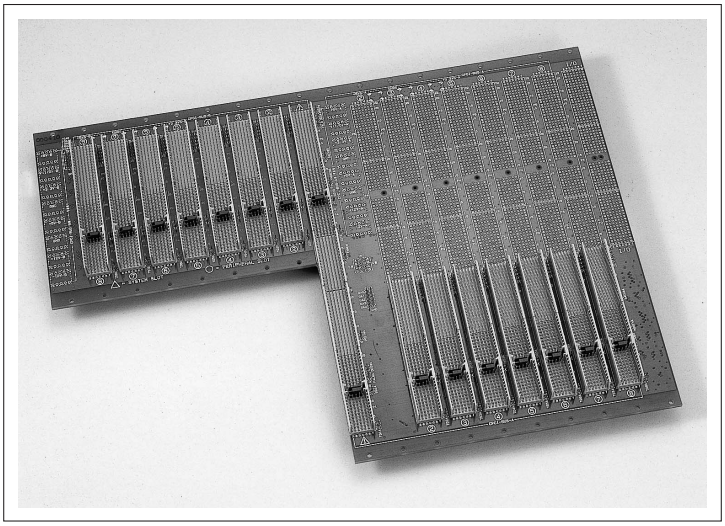


Component and connector side

Solder side

Dual-Bus-Compatible 6U Backplane

A backplane designed for use with a dual-bus system



Relevant Specification

- PICMG2.1R1.0
- PICMG2.7D0.5

Product Features

- Bus A and bus B are arranged left to right to realize 16 physical slots.
- A 3U backplane can be implemented at the bottom surface for bus B.
- Use of this backplane with the dual-bus system rack is effective for applications that handle high-volume data or perform multiple processing since it has 14 CompactPCI slots. It meets many needs in industrial control applications. Combining 3U board slots and 6U board slots produces such merits as reduced man-hours, cost and increased slot availability.

ORDER CODE

CPCI-D-16S-6UR

- 6U board position R : Right
- No. of physical slots 16 : Sixteen
- Type : Dual-bus-compatible backplane compliant with PICMG2.7D0.5

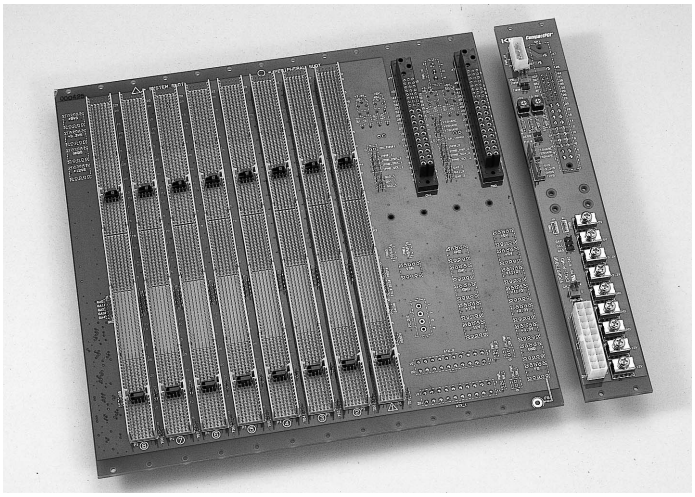
Product Specification

- Dual-width-slot backplane with built-in bridge board.
- Power supply layer for CompactPCI bus A is independent from that for CompactPCI bus B.
- Up to 14 peripheral boards can be used.
  System slot : 1
  Peripheral slot : 14 (seven 6U size boards for bus A and seven 3U size boards for bus B)
- Connectors P3, P4, and P5 on the bus-A side are for user-defined I/Os.
- Connectors P4 and P5 on the bus-B side are for the CompactPCI bus.

Unit:mm(inch)

Component side

A CompactPCI backplane compliant with plug-in power supplies



Relevant Specification

- PICMG2.0R3.0
- PICMG2.11R1.0
- PICMG2.9R1.0

Product Features

- The rear housings for connectors RP3 and RP5 are the AB types.
- Backplane allows jumper settings for future compliance with the PICMG2.9 specification.
- Ground and Frame ground connections are possible with short bar.
- Being compliant with the PICMG2.0R3.0 specification, this product is compatible with hotswappable backplanes.

ORDER CODE

CPCI-P-8S-R

- System slot position
  R : Right
- No. of slots
  8 : Eight
- Type : PICMG2.11R1.0 (compliant backplane compatible with plug-in power supplies)

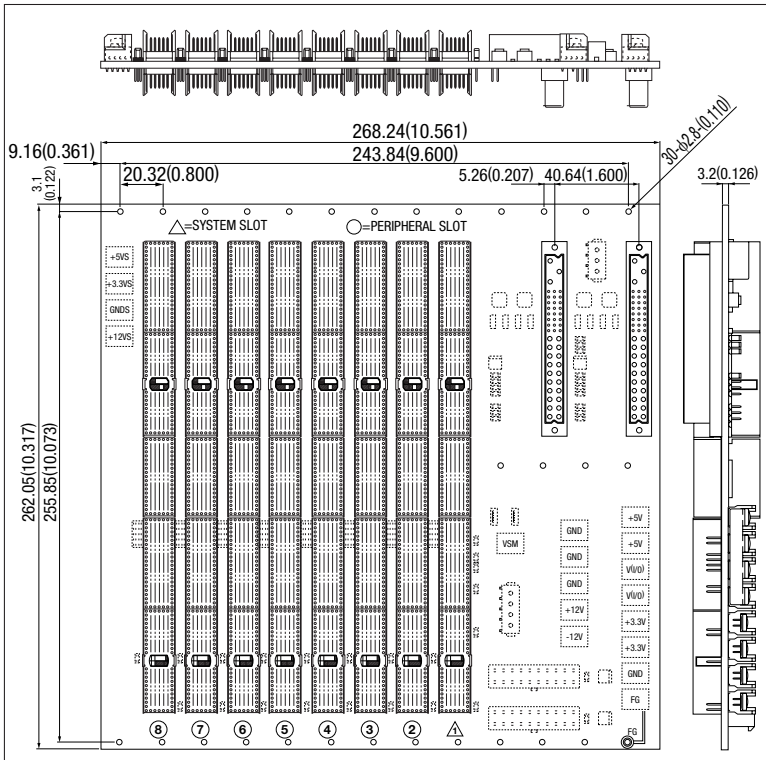
CPCI-P-MD

- MD : Module
- Type : PICMG2.11R1.0 (compliant backplane compatible with plug-in power supplies)

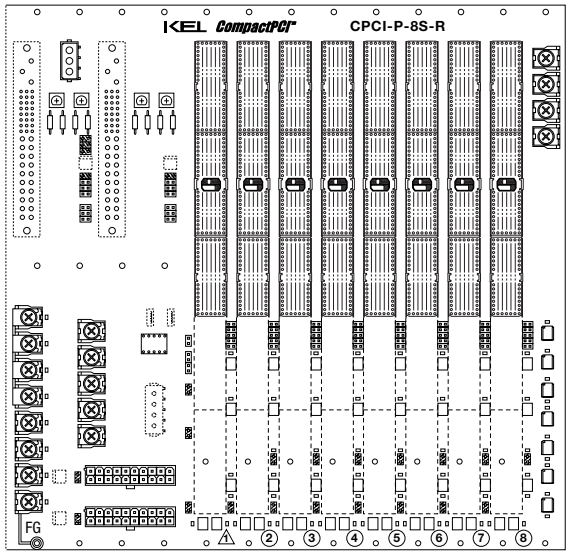
Product Specification

- Designed for use with the CPCI-PS-02 plug-in power supply unit.
- Complies with the PICMG2.0R3.0 specification.
- Connectors P3, P4, and P5 are for user-defined I/Os.
- Can be fitted with an optional Interlifent Platform Management Bus (IPMB) connector.
- Two ATX power supply connectors are fitted.
- Can be supplied with a floppy disk drive power supply connector (optional).
- Sensing point is located near the center of the board.
- Can accommodate parallel operation of two plug-in power supply units.

Unit:mm(inch)

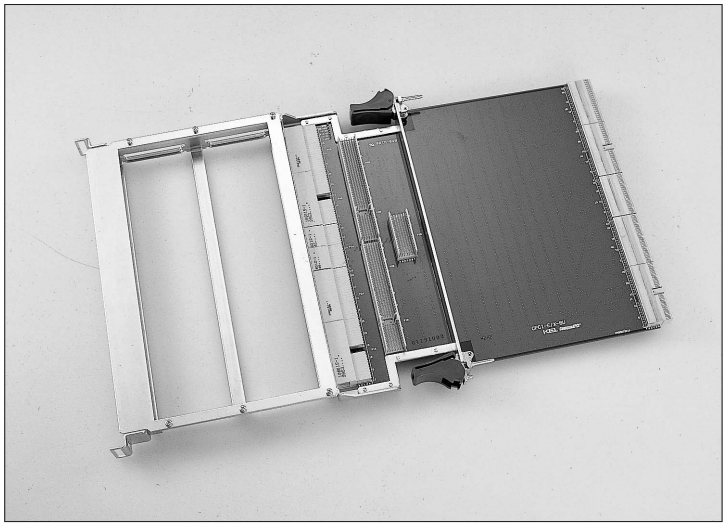


Component side



Solder side

A board used for extension of CompactPCI boards



Relevant Specification

- PICMG2.0R2.1

Product Features

- Extension Board can be inserted into or removed from a subrack easily using an ejector.
- Can be easily inserted into or removed from a test board chassis.
- Probe test is possible for all signals and power supply voltages.
- Probe test can be performed on the back of the extension board.

Product Specification

- 1.6mm-thick, eight-layer board.
- Pattern wiring was made as short as possible taking the stub length of CompactPCI boards into consideration.
- P3, P4, and P5 connectors are all parallel-wired.
- Chassis is made of SPCC.

Note:
This product satisfies the PICMG2.0R2.1 specification in terms of function. Given the product's purpose, however, the product does not satisfy the specification in terms of stub length. Users are requested to bear this fact in mind when confirming system operation.

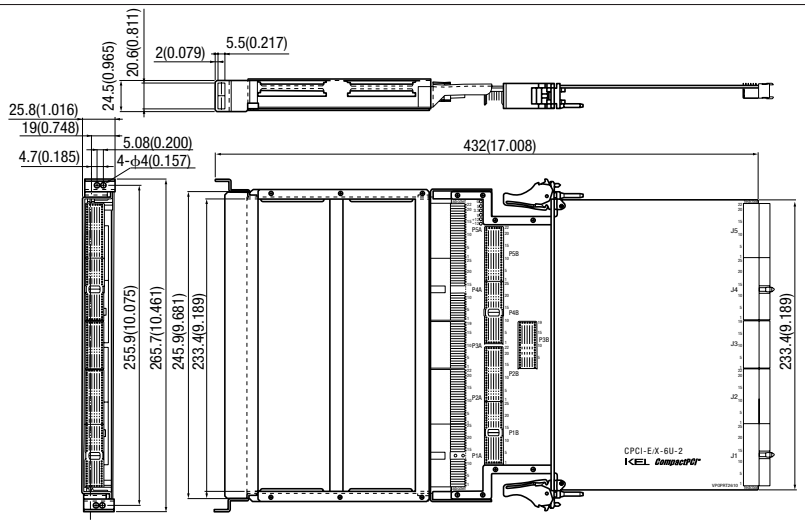
ORDER CODE

CPCI-E/X-□U-□

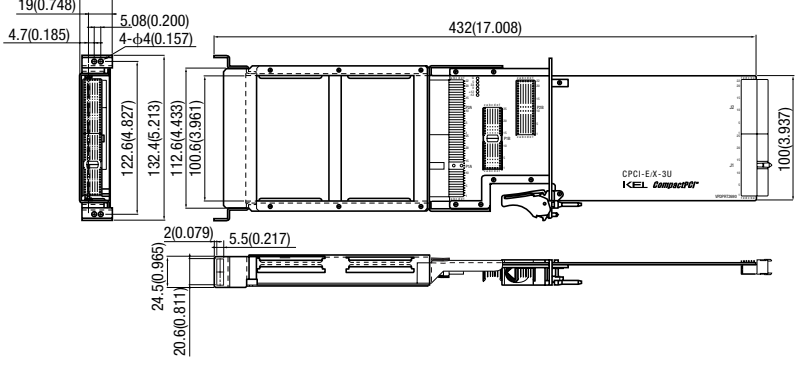
- Connector specification
  - Omit : Only J1 and J2 connectors are pre-mounted
  - 1 : Only J1, J2, J4 and J5 connectors are pre-mounted (6U)
  - 2 : All connectors J1 to J5 connectors are pre-mounted
- Board size
  - 3 : 3U (100mm)
  - 6 : 6U (233.35mm)
- Type : Extension board

Unit:mm(inch)

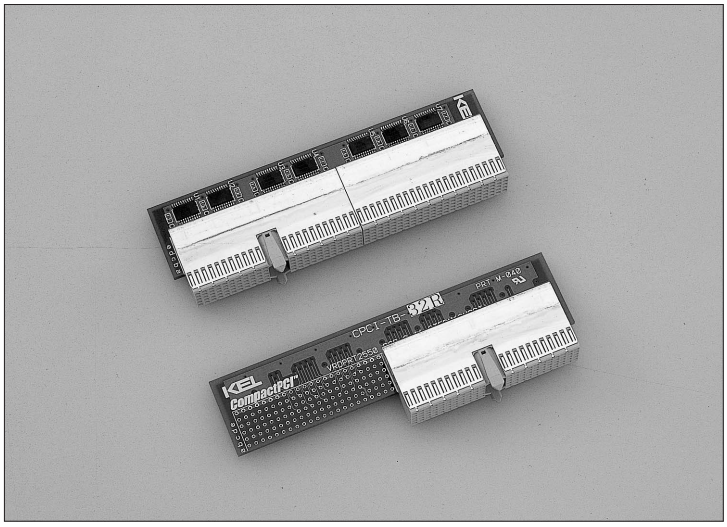
CPCI-E/X-6U-2



CPCI-E/X-3U



A bus termination board with diode array



Relevant Specification

- PICMG2.0R2.1

Product Features

- This termination board clamps bus-line overshoots and undershoots in light-load applications using an eight-slot backplane.
- This product is designed for use with the CPCI-8S-□T-R2.1 backplane (see page M-6).

Product Specification

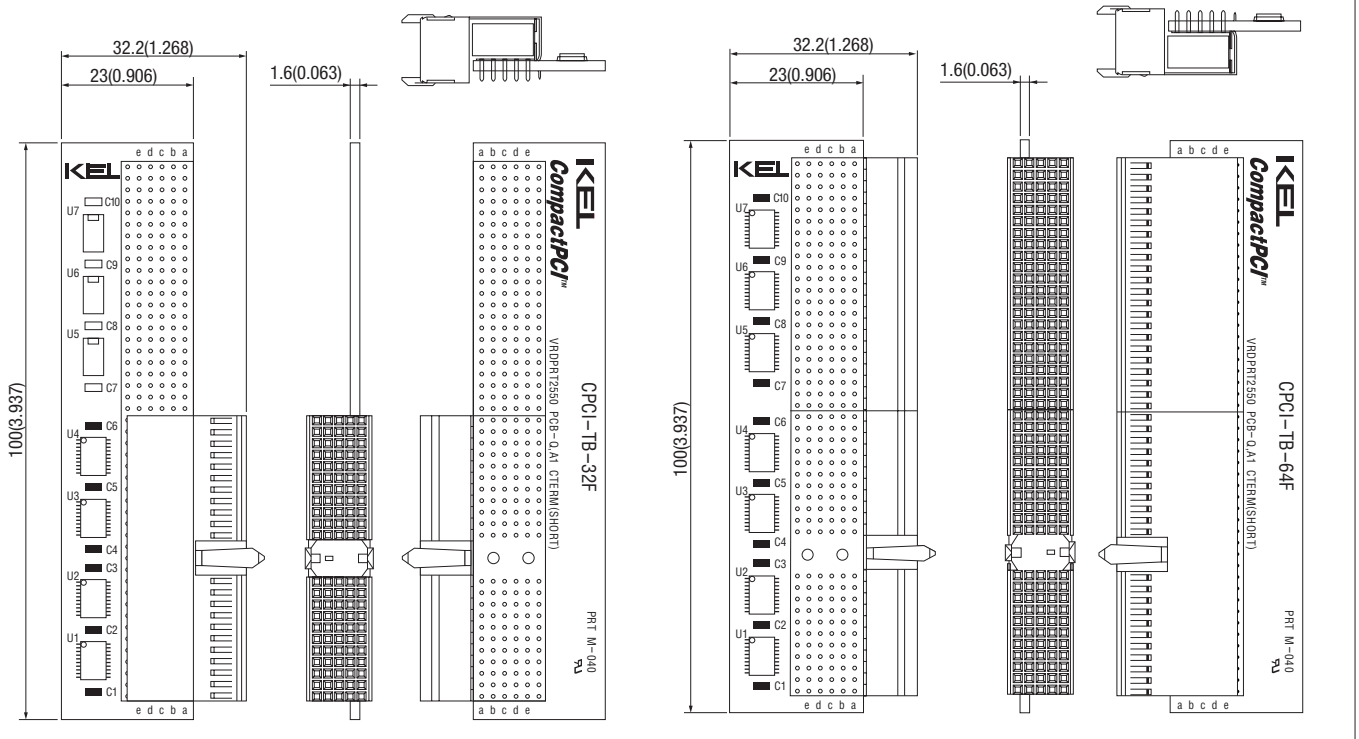
- 1.6mm-thick, four-layer board.
- Fitted with a 74S1053 diode array
- Can be used in both 5V and 3.3V signal environments.
- Insertion is possible from the front and rear.
- 64-bit and 32-bit types are available.

ORDER CODE

CPCI-TB-□□-□

- Insertion
  R : From rear F : From front
- Applicable system
  32 : 32-bit 64 : 64-bit
- Type
  Termination board

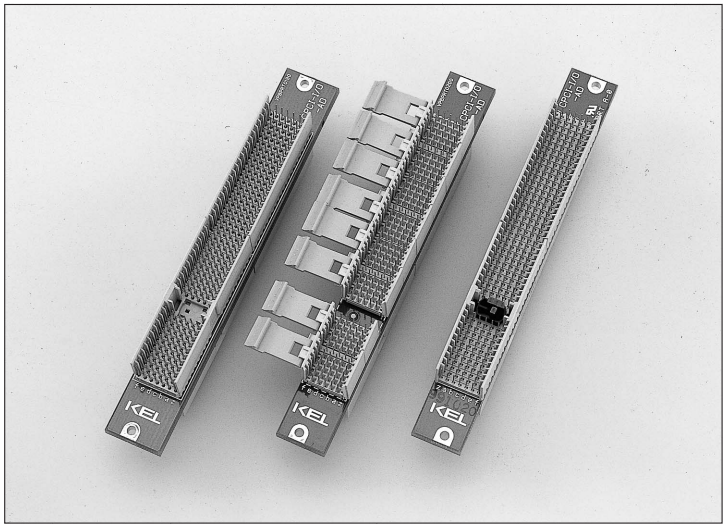
Unit:mm(inch)



CPCI-TB-32F

CPCI-TB-64R

A adapter board for user-defined I/Os



Relevant Specification

- PICMG2.3R1.0
- PICMG2.4R1.0

Product Features

- Used with a 3U backplane, this adapter board allows configuration of user-defined I/Os with the user's desired number of slots.

Product Specification

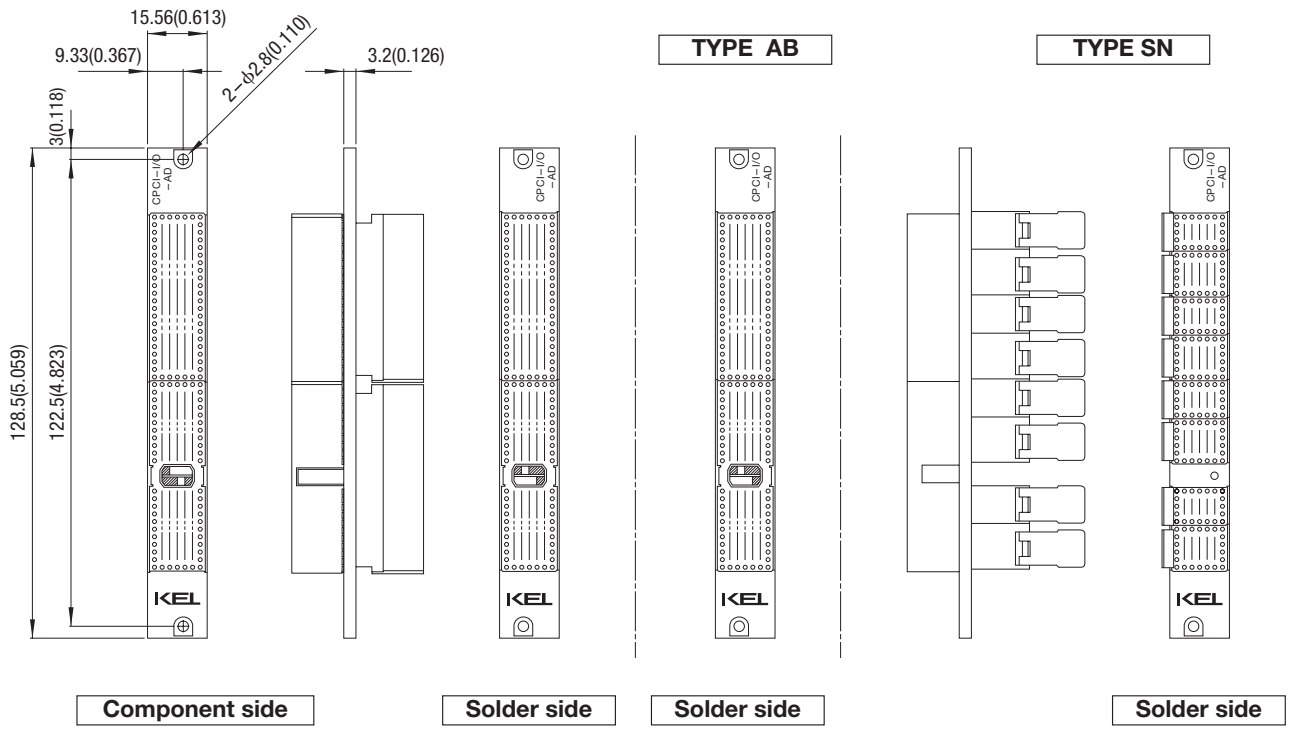
- 3.2mm-thick, dual-sided board.
- Rows f and z are for GND connection : all other rows are feedthroughs.
- The version with a snap latch can be used in a cableconnected configuration.
- Keying mechanism for user-defined I/Os is implemented in the P4 connector.

ORDER CODE

CPCI-I/O-AD-□□

- Type of RP5 housing
  - Omit : PICMG2.0R2.1 compatible (type B)
  - SN : With snap latch
  - AB : PICMG2.0R3.0 compatible (type AB)
- Type I/O-AD : Adapter for I/Os

Unit:mm(inch)



Comparison of PICMG2.0R2.1-Compliant Bus and PCI Bus

[Additions]
①Two power supply status signals
②Two IDE interrupt support signals
③One each of SYSTEM#, EMUM# and M66EN# signals
④Five geographical addressing signals for JTAG testing
⑤11 power supply V (I/O) signals
⑥Signal lines CLK0-CLK6, REQ0#-REQ6#, and GNT0# -GNT6# (seven each)

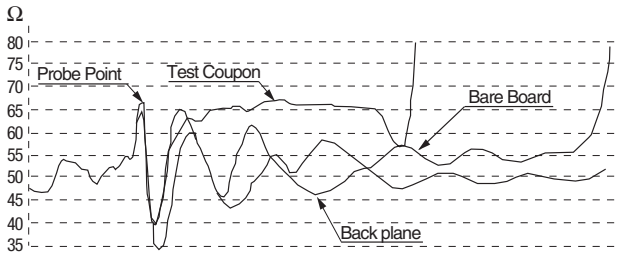
[Other Changes]
Although the PCI Specification defines the PRSET1# and PRSET2# signals, the PICMG2.0R2.1 specification defines only one PSET1# signal

[Key Features]
A PCI bus exists on a motherboard, enabling controllers to be connected to PCI slots directly by non-bus wiring. A CompactPCI bus, on the other hand, uses a backplane, which makes it necessary for all wiring to be included in the bus itself. Typical signals becoming necessary to be bussed in a CompactPCI system are CLK, REQ#, and GNT#. One each of these signals is necessary with a PCI bus, but seven each (CLK0-CLK6, REQ0#-REQ6#, and GNT0#-GNT6#) are necessary with a CompactPCI bus. In other respects concerning signals, a CompactPCI bus exactly the same as a PCI bus.

Electrical Characteristics of CompactPCI Bus

CompactPCI buses Uses PCI devices that comply with the PCI Specification. Unlike conventional buses, PCI buses use the reflection termination technique, which precludes the need for separate signal termination devices. With a CompactPCI bus, however, a10(stub) termination resistor (damping resistor) and a diode array are necessary owing to increases in the number of slots and other factors. Further, two different signaling environments (5V and 3.3V) are defined with a CompactPCI bus. Implementation of necessary measures is essential when 5V and 3.3V systems are used concurrently.

Characteristic Impedance

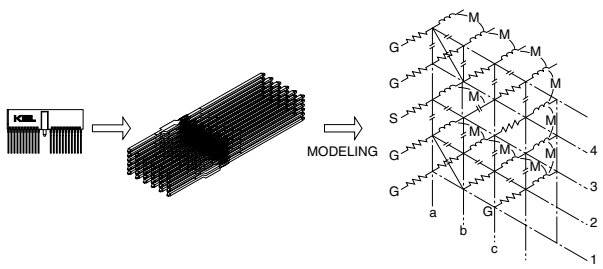


The diagram on the left shows the characteristic impedance curves of a single-bus test coupon of a KEL product and the bus line measurement results (Technical Data Report) obtained with one of KEL's CompactPCI board products. In general, the bus charactersristic impedance varies greatly depending on the connector through-hole, the mounted connector's floating capacity, and the presence or absence of capacitive load accompanying insertion and removal of the board. In light of these factors, the PICMG2.0R2.1 specification requires a 65Ω ±10% characteristic impedance for a single-bus line. All KEL CompactPCI products are designed to meet this requirement.

Cross-talk

The PICMG2.0R2.1 specification does not clearly define requirements for undesired Cross-talk effects that are inherent in certain motherboard layouts. It is known that Cross-talk has a greater influence on the connector than on the board. All boards of KEL's products incorporate Cross-talk-reducing measures such as distribution of adjacent signal, lines to different layers and creation of shields between patterns by grounding, so the characteristic impedance and other characteristics are not disturbed by Cross-talk effects.

Connector Circuit Model



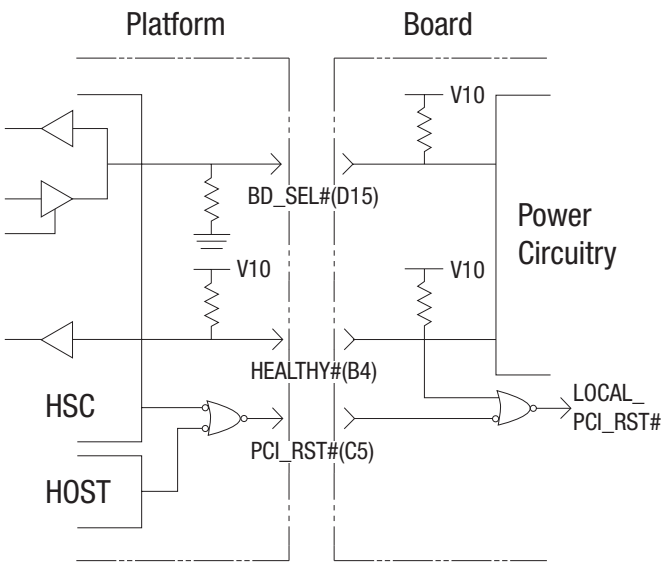
The PICMG2.0R2.1 specification requires every connector manufacturer to provide a circuit model for every connector. All manufacturers use almost the same basic methods for modeling their products, such as transmission line modeling or distributed constant modeling with the resistance, inductance and capacitance established. Connector modeling, however, is a hard job, especially for a connector requiring a high level of precision. In modeling such a connector, the influence of assigning signals to adjacent pins and ground shielding must be taken into consideration. KEL makes SPICE models of its products using parameter values extracted from many measurements. Also, we are preparing to enable customers to perform simulations using models downloaded from our Web site.

System	Hardware Connection	Software Connection
Basic Hot Swap system	Automatic by Hardware	Manual by Operator
Full Hot Swap system	Automatic by Hardware	Automatic Control by Software
High Availability system	Control by Software	Automatic Control by Software

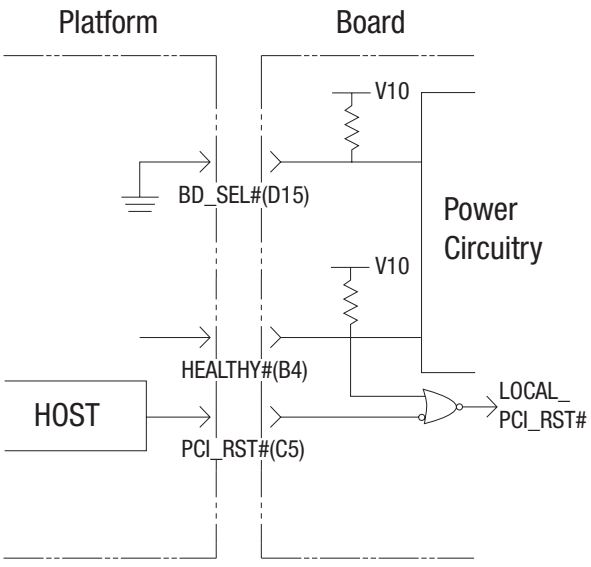
System	Board type	Platform type
Basic Hot Swap system	Basic Hot Swap board	Hot Swap platform
Full Hot Swap system	Full Hot Swap board	
High Availability system	Basic Hot Swap board	High Availability platform
	Full Hot Swap board	

- Hardware Connection Control
  3 signals, BD_SEL#, HEALTHY#, PCI_RST# are controlled by software using Hot Swap Controller.
- Software Connection Control
  Support by Hot Swap Control and Status Bit (EIM, LOO, INS, EXT), ENUM#, Blue LED, Handle Switch is requested.

Hardware Connection Control



No Hardware Connection Control



A CompactPCI Glossary

[ATX specification]
■ A specification proposed by Intel for the layout of personal-computer components. It is different from the AT specification in several respects.

[Bridge IC]
■ Any of several types of IC used to connect different buses when bus expansion is impossible by electrical means.

[Characteristic impedance]
■ The impedance of a transmission line such as a cable or wiring on a board. A characteristic impedance of 65 ±10% is defined in the CompactPCI Specification.

[Configuration space]
■ A memory area reserved for implementation of board hot-swap capability by means of software. It stores address and interrupt settings for hot swapping that were previously made manually using DIP switches.

[Decoupling capcity]
■ A capacitor provided on power supply line to reduce noise caused by simultaneous switching and other factors. The CompactPCI Specification defines detailed requirements for its values and location.

[Dual system]
■ The CompactPCI Specification defines a method for making a single backplane accommodate two CompactPCI buses by implementing two bridge ICs in the primary PCI bus on a CPU board. The bus on the side of connectors P1 and P2 is called bus A, and that on the side of connectors P4 and P5 is called bus B. Connector P3 is given standardized pin assignment for individual I/Os. Defined for these I/Os are eight interfaces, i.e., IDE Disk Interface, Floppy Disk Interface, Serial Channels (Com1 and Com2), Universal Serial Bus (USB), Printer port (LPT1), PS/2 Mouse and Keyboard Interface, Push-Button Reset input, and Push-Button NMI input.

[ECTF (Enterprise Computer Telephony Forum)]
■ An American consortium of companies related to computer telephony. The specification of the H110 bus is developed and controlled by the FCTF.

[Embedded system]
■ A mechanism provided on a connector or guide rail to prevent an incorrect board from being inserted. Insertion of an incorrect board is one of the primary causes of system malfunctions.

[EMC]
■ The capability of electronic equipment to provide its intended function without causing or suffering intolerable electromagnetic disturbance.

[EMI]
■ Unwanted elelctromagnetic radiation or noise in radio frequency band.

[ESD]
■ Discharge of high-voltage static electricity harmful to electronic equipment. Caused mainly by lightning or an electric charge accumulated on a human body.

[Eurocard]
■ The specification adopted in the VME and Multibus II specifications primarily for racks and boards produced in compliance with the relevant IEEE and IEC standards.

[Hot Swap]
■ Functionality allowing removal/insertion of a board without power-off of system, similar to the functionality known as "plug and play" with the PCI bus.

[Interrupt signal]
■ A signal used by a board to request the CPU's immediate attention. In a CompactPCI system, interrupt capability is implemented for eight slots by circulation of four PCI signals INTA#-ID#.

[IP(ANSIVITA 4-1995 IP Modules)]
■ An IP module implemented on a board. The PICMG2.3R1.0 specification defines its pin assignment on a CompactPCI board.

[IPMI]
■ The specificaiton defining a management bus standardized by Intel, Hewlett-Packard, NEC, and Dell in December 1999. The bus is incorporated in the PICMG2.9 specification together with the I2C bus.

[I2C]
■ A serial bus defined by a Philips specification. It is expected to be incorporated in the PICMG2.0R2.9 specification. The bus is also expected to be expanded in the future PICM2.0R3.0 specification.

A CompactPCI Glossary

[JTAG (Joint Test Action Group)]

■ A group supporting the ISP (developed to overcome the limitations of conventional incircuit testing) and the Boundary Scan test. These testing methods are defined by the IEEE 1149.1 standard and currently applied to many devices.

[Keying]

■ A mechanism provided on a connector or guide rail to prevent an incorrect board from being inserted. Insertion of an incorrect board is one of the primary causes of system malfunctions.

[Pallet type bridge]

■ The CompactPCI Specification defines several types of bridges. The pallet-type bridge makes horizontal connection from the back to the side of a backplane. Other bridge types include the front bridge and rear birdge.

[PCI bus]

■ A bus of 32-bit/64-bit data width, 33MHz/66MHz sychronizing clock frequency, and 5V/3.3V power supply voltage. It has attracted most attention in desktop computer applications.

[PCISIC (Peripheral Component Interconnect Special Interest Group)]

■ A consortium of manufacturers controlling the PCI bus specifications. The PCI-X bus, a next-generation PCI bus supported by the PCISIG, is attracting much attention.

[Peripheral slot]

■ All the slots other than the system slot in a CompactPCI backplane are called peripheral slots. They are identified by circles around their slot numbers.

[PICMG]

■ A consortium of companies involved in utilizing the PCI bus, which was created for desktop-computers, in industrial applications.

[PMC (PCI Mezzanine Cards IEEE P1386.1)]

■ The specification defining PCI Mezzanine cards.

[Primary side]

■ When two CompactPCI buses are connected using a bridge IC or by other means, the higher-ranked bus is called the primary-side bus and the lower-ranked bus is called the secondary-side bus.

[PXI Bus]

■ A CompactPCI bus for instrumentation and control applications proposed by National Instruments. It is similar to the VXI bus, which is a VME bus defined by Hewlett Packard.

[Rear I/O board]

■ A board inserted from the rear of a backplane defined by the IEEE1101.11. In the CompactPCI Specification, a board depth of 80 mm is defined.

[Ripple voltage]

■ The alternating component of a direct-current power supply unit's output. According to the definition of the CompactPCI Specification Revision 2.1, it must be limited to ±50mV.

[Synchronous system]

■ A bus system with an internal clock by which transmission time is defined. A bus system without a clock is called an asynchronous system. A CompactPCI bus system is a synchronous system. Theoretically, asynchronous systems are more suitable for high-speed transmission than synchronous systems but designing a high-speed system with asynchronous buses is more difficult than designing one with synchronous buses. For this reason, synchronous buses are now used more widely in high-speed systems. Versa Module European (VME) buses are asynchronous buses.

[System slot]

■ A slot in a CompactPCI backplane in which the bus's principal, controlling board is inserted. The system slot is located at the left-or right-hand side of the backplane. The system slot board is generally a CPU board. The system slot is identified by a triangle around its slot number.

[Transaction]

■ A term used to describe a basic bus operation irrespective of the kind of access (such as address phase and data phase). The term "bus cycle" is also used.

[VCCI (Voluntary Control Council for Interference by Information Technology Equipment)]

■ The Japanese Electromagnetic Interference Controlling organization. Its main activity is controlling the VCCI standard in accordance with the CISPR Pub. 22.

A CompactPCI Glossary

[Versa Module European(VME) bus]

■ The Motorola 68000-series VERSA bus defined by the IEC821 and IEEE1014-87 standards. It is the most widely used bus in industrial applications.

[VITA (VMEbus International Trade Assoc.)]

■ The organization responsible for control and establishment of VME specifications.

[VME64]

■ A 64-bit-data-width version of the VME bus. It is defined by a specification established in February 1995.

[VME64x]

■ A version of the VME64 bus whose specificaiton additionally includes, such requirements as a 3.3V power supply, rack dimensions conforming to IEEE1101.1,10, and 11, and 2mm HM connector. It is defined by a specification established in January 1997.

PICMG CompactPCI Specifications and KEL CompactPCI Products (as of May 8, 2000)

Each PICMG CompactPCI Specificaiton number takes the form "PICMG2.□D□.□" or "PICMG2.□R□.□". The part in the form "PICMG1.□" is the PICMG bus number. A suffix of the form "D□.□" indicates a draft specificaiton, and a suffix of the form "R□.□" indicates an officially released specification. The higher number is the later revision.

■ PICMG2.0R2.1 CompactPCI Specification (September 2,1997)
This is the core CompactPCI specification. Most currently produced CompactPCI boards comply with it. Revision 2.1 will remain the core CompactPCI specification until it is replaced by Revision 3.0. •••CPCI-□S-□-R2.1 (M-9)

■ PICMG2.0R3.0 CompactPCI Specification (August 1,1999)
This is the latest revision of the CompactPCI Specification. It contains many definitions promoting compatibility with PICMG2.1R1.0. Revision 3.0 is expected to become the core CompactPCI specification in place of Revision 2.1. It includes definite specifications for 66MHz bus clock frequency systems. •••CPCI-P-8S-R (M-17)

■ PICMG2.1R1.0 CompactPCI Hot Swap (May 14,1998)
This specification defines requirements for hot-swap capabilities. •••CPCI-H-□S-□ (M-12)

■ PICMG2.2R1.0 VME64x on CompactPCI (August 7,1998)
This specification defines requirements for VME64x/CompactPCI hybrid system backplanes.

■ PICMG2.3R1.0 PMC on CompactPCI (August 7, 1998)
This specification covers assignment of PIC Mezzanine Cards (PMCs) to user I/O pins (P3, P4, and P5 connectors).

■ PICMG2.4R1.0IP on CompactPCI (August 7 1998)
This specificaition covers assignment of IPs to user I/O pins (P3, P4, and P5 connectors). •••CPCI-I/O-AD-□□ (M-20)

■ PICMG2.5R1.0 CompactPCI Computer Telephony Specification (April 3, 1998)
This specification pertains to computer telephony. It uses the H.110 bus. •••CPCI-C-□S-R (M-13)

■ PICMG2.6D0.1 Bridging Beyond Eight Slots: Common Practices (March 25, 1999)
This specification pertains to common practices for expansion of bus slots using PCI-to-PCI bridge IC boards.
•••CPCI-B-15S-□-R (M-14)
•••CPCI-B/B-□□-□ (M-15)

■ PICMG2.7D0.56U Dual System Slot Specification (September 4, 1998)
This specification defines the method for enabling two CompactPCI buses to exist on a CPU boards.
•••CPCI-D-16S-6UR (M-16)

■ PICMG2.8D0.6 Instrumentation Subcommittee Pin Registration for PXI (November 20, 1998)
This specification pertains to the National Instruments PXI bus for instrumentation and control applications.

■ PICMG2.9R1.0 System Management Specification (February 2, 2000)
This specification defines requirements for using the Philips I2C serial bus. •••CPCI-P-8S-R (M-17)

■ PICMG2.10R1.0 Keying of CompactPCI Boards and Backplanes (August 1, 1999)
This specification defines the keying mechanism to be implemented with CompactPCI boards and backplanes.

■ PICMG2.11R1.0 Power Interface Specificaiton (August 1, 1999)
This specification pertains to CompactPCI plug-in power supplies and power connectors. •••CPCI-P-8S-R (M-17)
•••CPCI-PS-02

■ PICMG2.12D0.75 Hot Swap Infrastructure Interface Specification (April 3, 2000)
This is a draft specification. It apparently defines speicifications of infrastructure software for hot-swap capability that are not covered by the PICMG2.1R1.0 specification. It will include the specifications of the Windows NT Family of operating systems.

■ PICMG2.13D0.0 Redundant System Slot
This specification pertains to system-slot redundancy. As the revision number R0.0 indicates, this specification is still under review.

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■ The information in this brochure is subject to change without notice.
Please feel free to contact your local sales office for all technical supports.